Amphenol SOCAPEX

PS SERIES PSVD3UU48P600-X

VPX DC/DC POWER SUPPLY



- VITA 62 compliant
- 3U VPX form factor
- DC/DC converter
- 6 outputs
- 600W (700W peak)
- Current Share for VS# Outputs

- Input Options:
 - MIL-STD-704
 - MIL-STD-1275

Over 20 M Ω at test voltage:

200V between Input and Output

200V between Input and Case

100V between Output and Case

- Protocol VITA 46.11
- Cyber secure

Electrical Specifications

DC Input

18 to 48 V_{DC} *Max Non-Operating 100V*Options:

- 1) MIL-STD-704 (A-F) Normal and Abnormal Steady State
- 2) MIL-STD-704(A-F) transients Up to 50V, 80V
- 3) MIL-STD-1275 Surge
- 4) Def Stan 61-5 170V Load dump.

DC Output

VS1: 12V up to 30A VS2: 3.3V up to 20A 5V VS3: up to 30A 12V_Aux: 12V up to 1A -12V_Aux: -12V up to 1A 3.3V_Aux: 3.3V up to 5A

Peak power option:

VS1: 12V up to 40A VS3: 5V up to 35A

Current Sharing

Optional for VS1, VS2, VS3

Line/Load regulation

See Table 2 on page 7

Efficiency

Up to 88% 85.5 % @ Full Load (See Para. 4)

Ripple and Noise
Typically, less than 50mV_{P-P}
(max.1%_P). Measured across a 0.1μF capacitor and 10μF capacitor on load at Input Voltage of 18V-36V, all Temperature Range.

(See Para. 4)

<u>Load Transient Overshoot</u>

and Undershoot
Output dynamic response of less
than5% at load Step of 30%-60%.
Output returns to regulation in less
than 1mSec

Complies with MIL-STD-461F^{1 2} (5μH LISN²): CE101, CE102, CS101, CS114, CS115, CS116

System Management

VITA 46.11 Tier I IPMC Data Available:

- Output voltages and currents
- Input voltage
- Card Temperature
- Card Status

Notes

1. Compliance achieved with $5\mu H$ LISN, shielded cable and static resistive load.

Markets & Applications



Military: airborne, ground-fix, shipboard



Ruggedized, Telecom, Industrial Power Supply

Environmental 1

Design to Meet MIL-STD-810G

Temperature

Operating: -55 °C to +85 °C

at unit edge

Storage: -55 °C to +125 °C

Fungus

Does not support fungus growth, in accordance with the guidelines of MIL-STD-454, Requirement 4.

<u>Altitude</u>

Method 500.5, Procedure I & II Storage/Air Transport: 40 kft Operation/Air carriage: 70 kft

Humidity

Method 507.5, Up to 95% RH

Salt Fog:

Method 509.5

Shock

Method 516.6 40g, 11msec saw-tooth (all directions)

Vibration

Vibration: Figure 514.6E-1. General minimum integrity exposure. (1 hour per axis.)

Reliability: 305,000 Hours, calculated IAW MIL-HDBK-217F Notice 2 at +65°C, GF.

Note 1: **Environmental Stress Screening (ESS)** Including random vibration and thermal cycles is also available. Please consult factory for details.

Protections *

Input

Input Reverse Polarity:

Protection for unlimited time

Inrush Current Limiter

Peak value of 5 x I_{IN} for initial inrush currents lasting more than 50 µSec.

Under Voltage

Unit shuts down when input voltage drops below 17± 0.5VDC. Automatic restart when input

voltage returns to nominal

range.

Over Voltage Lock-Out

Unit shuts down when input steady state voltage rise above 55 ± 2VDC. Automatic restart when input voltage returns to nominal range.

Output

Passive over voltage protection on Aux outputs

Zener selected at 25% ± 5% above nominal voltage, is placed across the output for passive voltage limit.

Active over voltage protection on VS# outputs

20% ± 5% above nominal voltage.

Automatic recovery when output voltage drops below threshold.

Overload / Short-Circuit **Protection**

Continuous Hiccup protection (110-130%) for VS#. Aux Typical:

3.3Vaux / 8A 12Vaux. 1.5A-2A

-12Vaux. 2.5A-3A

General

Over Temperature Protection

Automatic shutdown at temperature of 95 ± 5 °C (at unit edge) Automatic recovery when temperature drops below 90 ± 5 °C.

Note 1: Thresholds and protections can be modified / removed (please consult factory)

Functions and Signals - According to VITA 62

Signal No.	Signal Name	Туре	Description
1	FAIL*	Output	Indicates to other modules in the system that a failure has occurred in one of the outputs. Please refer to Figure 2
			This signal is referenced to SIGNAL RTN .
2	SYSRESET*	Output	Indicates to other modules in the system that all outputs are within their working level. Please refer to Figure 2
			This signal is referenced to SIGNAL RTN .
3	INHIBIT*	Input	Controls power supply outputs. This signal in conjunction with INHIBIT controls the outputs. Please refer to Table 1 and Figure 1 This signal is referenced to SIGNAL RTN .
4	ENABLE*	Input	Controls power supply outputs. This signal in conjunction with INHIBIT controls the outputs. Please refer to Table 1 and Figure 1 This signal is referenced to SIGNAL RTN .
5	GA0*, GA1	Input	Used for geographical addressing. GA1 is the most significant bit and GA0 is the least significant bit. This signal is referenced to SIGNAL RTN .
6	SCL, SDA	Bidirectional	I2C bus Clock and Data respectively. Through this bus the voltage and temperature readouts can be shared. This signal is referenced to SIGNAL RTN .
7	REF_CLK	Input	The REF_CLK signal is used to allow the power supply frequency to sync with the system frequency. This signal is referenced to SIGNAL RTN .
8	VOUT SENSE	Input	The SENSE is used to achieve accurate load regulations at load terminals (this is done by connecting the pins directly to the load's terminals).
9	VS# SHARE	Bidirectional	Used for paralleling several PSVD3UU48P600-1 units (optional).
10	SIGNAL RTN	Gnd	Signal ground for all signal. Internally tied to output Power ground

Table 1 – Inhibit and Enable Functionality

INHIBIT*	Low	Low	High	High
ENABLE*	Low	High	Low	High
VS1 ,VS2,VS3, ±12VAux	OFF	OFF	ON	OFF
3.3V_AUX	ON	OFF	ON	OFF

Figure 1 – Inhibit and Enable Input stage

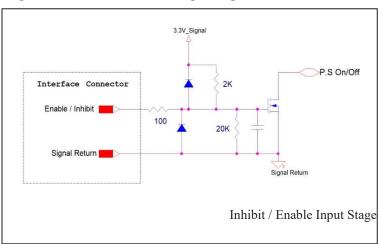
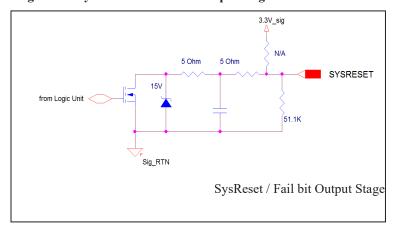
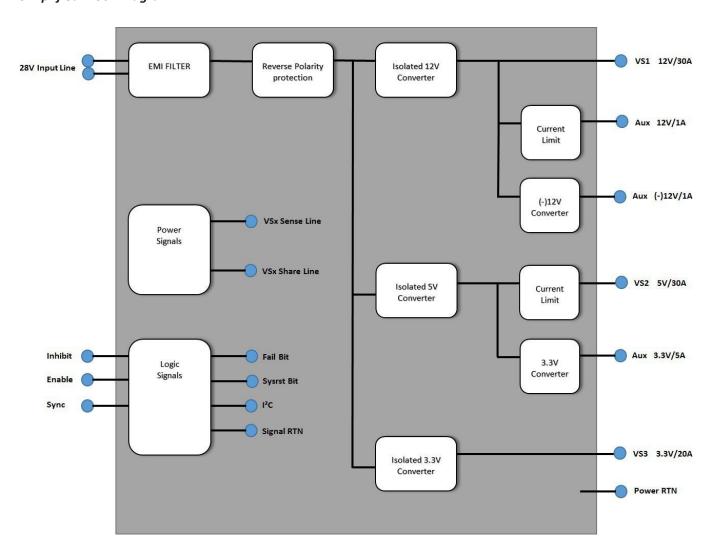


Figure 2 – SysReset and Fail Bit output stage



Simplified Block Diagram



Detailed Information

1. PSVD3UU48P600-X Input Voltage Operation Range.

The unit steady state operation voltage is 18V to 48V, continuously work up to 50V Input line. Unit can be modified to work up to 100V or down to 16V transient and Surge. Max Non operation Voltage 100V.

1.1 Low Line Turn-on and Turn-off Limits

To avoid Turn-on and Turn-off cycling glitch the unit have about 2V Hysteresis. The Turn-on threshold is under 20V and turn- off below 18V.

Those limits can be adjusted, contact Factory for more information.

2. Outputs Voltage Regulation

The PSVD3UU48P600-X contains accurate internal sense lines to keep output voltage at less than 3% regulation for all Line/ Load and temperature range (see Table 2).

Out	put	12V/25A	5V/30A	3.3V/20A	3.3VAux/5A	12VAux/1A	(-)12VAux/1A	Notes
Voltage Range		11.85 – 12.15	4.9 – 5.1	3.28 – 3.42	3.25 – 3.45	11.7 – 12.2	(-)11.85 – (-)12.15	
Voltage Range		11.80 – 12.20	4.9 – 5.2	3.20 – 3.40	3.25 – 3.45	11.7 – 12.2	(-)11.7 – (-)12.2	Current share configuration

Table 2: Outputs voltage regulation. VIN 18V – 48V, Temperature -55 °C – 85 °C single and parallel configuration.

2.1. Sense Lines

Sense Lines are provided for VS1, VS2 and VS3 output to compensate line voltage drop.

Sense Lines proper connection is shown in Figure 3.

Each VSx output has its own Sense Lines, additional common Sense RTN

Line is provided for all VSx Outputs (VITA 62 Standard).

Contact Factory for Sense configuration different than the VITA 62 standard

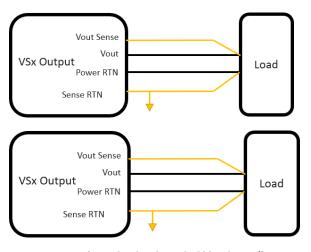


Figure 3: PSVD3UU48P600-X Sense line connection

3. Output Power

The PSVD3UU48P600-X can deliver up to 616W steady State at all temperature and input range. Unit can support a peak power of 700W, please contact factory for more details and limitations.

Max Total Power Output	12V/30A	5V/30A	3.3V/20A	3.3VAux/5A	12VAux/1A	(-)12VAux/1A
616W	30A	30A	20A	5A	1A	1A
700W	40A	35A	20A	5A	1A	1A

3.1 Current Sharing (Optional)

Current sharing is available for VS1, VS2 and VS3 outputs. Load share pins should be connected for Hiccup synchronization.

3.3Vaux and ±12V Aux can be safely paralleled. To obtain a good current sharing the following steps should be taken

- Connect hiccup pins of desired outputs to guarantee simultaneously Turn-on of paralleled outputs.
- Connect Sense Line of both paralleled outputs to the same point.
- Make sure Power traces are as identical as possible for both current sharing outputs.

3.2 Typical Efficiency (Typical results at room temperature)

Input Voltage	Output Power Efficiency		
	170W	88%	
28V	200W	87.6%	
	600W	86.1%	

4. Typical EMI Tests

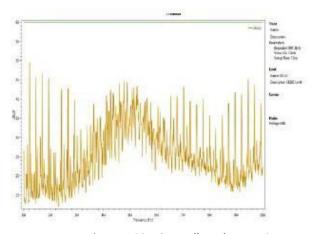
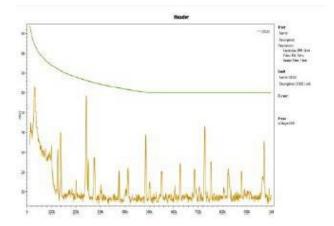


Figure 4: 28V Line, Full Load, 5UH LISN



5. IPMI Protocol

Electrical Parameters

Vcc: 3.3VDC Pull-up: 10K Ohm

Input Capacitance 330Pf

Slave Device Addressing

- 256 address spaces

- Baud rate: 200kHz maximum

- 7 Bit Protocol

- Support Slot Addressing per VITA 62

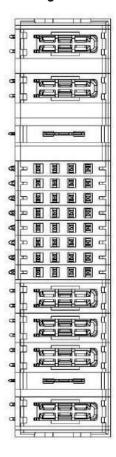
	MSB							LSB
Slot Number	A6	A5	A4	A3	A2	A1/*GA1	A0/*GA0	R/W
Slot0	0	1	0	0	0	0	0	
Slot1	0	1	0	0	0	0	1	
Slot2	0	1	0	0	0	1	0	
Slot3	0	1	0	0	0	1	1	

^{*} Slot location is determined by GAx per VITA 62.

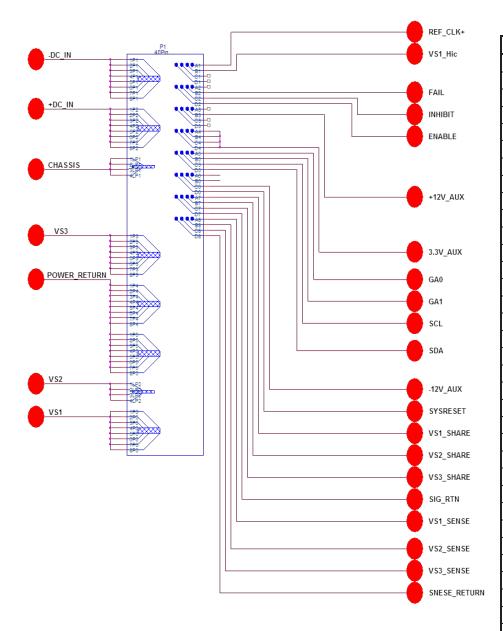
Communications Supported

Support 46.11 Tier 1 For additional information, please contact factory

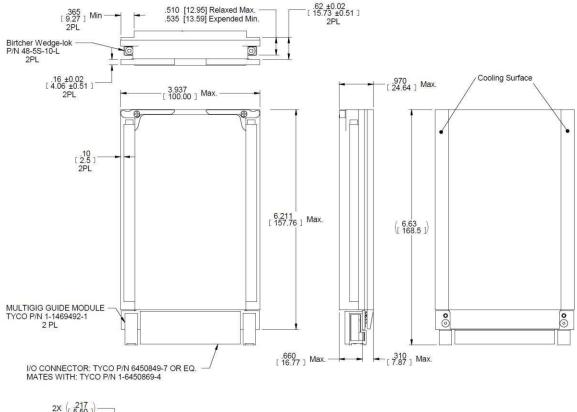
Pin Assignment

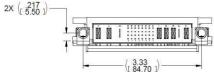


2ACP+ILP+32S+3HDP+ILP+IHDP	6450849-7				NOROCK N	DART NUMBER
S+3HD	A	В	C	D	0.00	DOWS
P+1L			=		ъ	2553
P+1		12	=		P2	POWER
-DP		-	7		P2 LP1	20
	05	R5	Y 5	25	-	
	05	R5	15	25	2	
	05	R5	75 Y5 Y5 Y5 Y5 Y5 Y5 Y5	25 25 25 25 25 25 25	ÇU	
	05	R5	Y 5	7.5	4	510
	0.5	25	7.5	15	C)	SIGNAL
	05	R5	3	25	on:	
	05	85	15	25	7	
	0	R5	15	25	00	
		8	Р3			
		83	4		P 4	_
		1	7		P.5	POWER
		_	7		P4 P5 LP2 P6	æ
			7		P 6	



Pin Number	Pin Name
P1	-DC_IN
P2	+DC_IN
LP1	CHASSIS
Р3	VS3
P4	POWER_RETURN
P5	POWER_RETURN
LP2	VS2
P6	VS1
A8	VS1_SENSE
B8	VS2_SENSE
C8	VS3_SENSE
D8	SENSE_RETURN
A7	VS1_SHARE
B7	VS2_SHARE
C7	VS3_SHARE
D7	SiG_RTN
A6	N.C
В6	N.C
C6	-12V_AUX
D6	SYSRESET*
A5	GA0*
B5	GA1*
C5	SCL
D5	SDA
A4	+3.3V_AUX
B4	+3.3V_AUX
C4	+3.3V_AUX
D4	+3.3V_AUX
A3	N.C
B3	+12V_AUX
C3	N.C
D3	N.C
A2	N.C
B2	FAIL*
C2	INHIBIT*
D2	ENABLE*
A1	REF_CLK+
B1	VS1_Hic
C1	N.C
D1	N.C





Notes

- 1. Dimensions are in Inches[mm]
- 2. Tolerance is:
 - $.XX \pm 0.02 IN$
 - .XXX $\pm~0.008~\text{IN}$
- 3. Weight: Approx. 796 g (28.08 oz)
- 4. 3D model available

Note: Specifications are subject to change without prior notice by the manufacturer.





